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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,984	12/28/2001	Yong Jin Cho	8733.563.00	3746

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EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,984	CHO ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims

Claims 1-12 are pending per Amendment of November 10, 2005 with claims 1-3, 5, 8 and 11 amended per said Amendment.

Priority

Priority to Korean Patent Application No. 2001-024581 (May 7, 2001) is claimed.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,668,379 (to Ono et al.)(Published Sept. 16, 1997)(To Hitachi, Ltd.) in view of United States Patent 5,825,449 (to Shin)(Published Oct. 20, 1998).

Regarding claim 1 (amended), Ono teaches and discloses in all embodiments an active matrix liquid crystal display device comprising a plurality of gate lines formed on an insulating substrate, a plurality of data lines formed so as to cross the plurality of gate lines, thin film transistors formed in the vicinity of respective intersections of the plurality of the gate lines and the data lines and pixel electrodes connected to the thin film transistor (Column 2, "Methods for Solving the Problems", Lines 23-30)(Applicant's "a plurality of gate lines on an insulating

substrate, a plurality of data lines, and a plurality of TFTs, the gate lines crossing the data lines to define a pixel region and the TFTs being formed at crossing points of the gate and data lines").

Turning to Figure 16, for example, Ono illustrates a contact hole (pixel electrode region) that electrically connects a source electrode (SD1) of the TFTs with a pixel electrode (d2) of the pixel region is formed over predetermined portions of the source electrode (SD1) and the pixel region and wherein the pixel electrode directly contacts the insulating substrate (SUB1 in pixel electrode region), the source electrode (SD1), and a gate insulating film (GI) contacting a gate electrode (GL (g1)).

Please note that the terms "drain" and "source" are conventionally used interchangeably. That is, drain = source and source = drain. Please see, for example, United States Patent 5,838,400 (to Ueda et al.)(Published Nov. 17, 1998)(to Hitachi, Ltd.)(stating "[i]t is, therefore, understood that the source electrode and the drain electrode are switched during operation ... polarity is fixed for convenience, with one of the electrodes taken to be a source electrode and the other a drain electrode.")(Column 8, Lines 53-61) ; See also, United States Patent 5,528,396 (to Someya et al.)(Published June 18, 1996)(to Hitachi, Ltd.)(stating "the source/drain is, it should be understood, interchangeable during the operation ... one is fixedly expressed as a source, and the other a drain for convenience.").

Ono does not appear to explicitly specify *exposing the insulating substrate through a gate insulating film and a passivation film*.

Shin teaches and discloses a liquid crystal display device and manufacturing method in which (Figure 5) a contact hole is formed through a gate insulating layer (3) and a passivation layer (9).

It would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Ono in view of Shin for fewer process steps (See Shin, Column 5, Lines 35-50).

Thus, claim 1 is rejected.

As to claim 2 (amended), the gate electrode (GL (g1)) is formed on the insulating substrate (SUB 1), the gate insulating film (GI) formed on the entire surface of the insulating substrate (SUB 1) including the gate electrode (GL (g1)), a semiconductor layer (AS) and an ohmic contact layer (d0) sequentially deposited at a predetermined portion on the gate insulating film (GI) and source and drain electrodes formed right and left (SD1 and DL) on the ohmic contact layer (d0).

Although not shown in Figure 16, a passivation film (PSV1) is formed over the thin film transistor for protecting the thin film transistor from moisture and other contaminants (Column 12, Lines 12-14). Also, please note that layer d1 in Figure 16 is made of chromium and thus a passivation film conventionally covers a chromium layer to protect the chromium film from corrosion. Please see, e.g., United States Patent 5,751,381 (to Ono et al.)(Published May 12, 1998)(to Hitachi, Ltd.)(Column 12, Lines 51-57)(Applicant's "a passivation film formed on the entire surface of the substrate including the source and drain electrodes, a contact hole formed by etching the passivation film to expose a predetermined portion of the drain electrode and a predetermined portion of the insulating substrate, where a pixel electrode will be formed later and the pixel electrode formed on the passivation film and the contact hole.").

Thus, claim 2 is rejected.

As to claim 3 (amended), Ono teaches and discloses in all embodiments an active matrix liquid crystal display device comprising a plurality of gate lines formed on an insulating substrate, a plurality of data lines formed so as to cross the plurality of gate lines, thin film transistors formed in the vicinity of respective intersections of the plurality of the gate lines and the data lines and pixel electrodes connected to the thin film transistor (Column 2, "Methods for Solving the Problems", Lines 23-30)(Applicant's "gate lines arranged to cross data lines on a substrate, thereby defining a pixel region; thin film transistors, each having a gate electrode and source and drain electrodes, formed at crossing points of the gate lines and the data lines;".)

Turning to Figure 16, for example, Ono illustrates a contact hole (pixel electrode region) that electrically connects a source electrode (SD1) of the TFTs with a pixel electrode (d2) of the pixel region is formed over predetermined portions of the source electrode (SD1) and the pixel region and wherein the pixel electrode directly contacts the insulating substrate (SUB1 in pixel electrode region), the source electrode (SD1), and a gate insulating film (GI) contacting a gate electrode (GL (g1)).

Please note that the terms "drain" and "source" are conventionally used interchangeably. That is, drain = source and source = drain. Please see, for example, United States Patent 5,838,400 (to Ueda et al.)(Published Nov. 17, 1998)(to Hitachi, Ltd.)(stating "[i]t is, therefore, understood that the source electrode and the drain electrode are switched during operation ... polarity is fixed for convenience, with one of the electrodes taken to be a source electrode and the other a drain electrode.")(Column 8, Lines 53-61) ; See also, United States Patent 5,528,396 (to Someya et al.)(Published June 18, 1996)(to Hitachi, Ltd.)(stating "the source/drain is, it

should be understood, interchangeable during the operation ... one is fixedly expressed as a source, and the other a drain for convenience.").

Thus, claim 3 is rejected.

As to claim 4, the contact hole of Figure 16 is formed over an edge part of the source electrode and the pixel region adjacent to an edge part of the source electrode.

Figure 16, shows the contact hole traced over part of the source electrode and into the pixel region.

Thus, claim 4 is rejected.

As to claim 5 (amended), the gate electrode (GL (g1)) is formed on the insulating substrate (SUB 1), the gate insulating film (GI) formed on the entire surface of the insulating substrate (SUB 1) including the gate electrode (GL (g1)), a semiconductor layer (AS) on the gate insulating film (GI) above the gate electrode (GL(g1)), source (SD1) and drain (DL) electrodes located at opposite sides of the semiconductor layer (AS).

Although not shown in Figure 16, a passivation film (PSV1) is formed over the thin film transistor for protecting the thin film transistor from moisture and other contaminants (Column 12, Lines 12-14). Also, please note that layer d1 in Figure 16 is made of chromium and thus a passivation film conventionally covers a chromium layer to protect the chromium film from corrosion. Please see, e.g., United States Patent 5,751,381 (to Ono et al.)(Published May 12, 1998)(to Hitachi, Ltd.)(Column 12, Lines 51-57)(Applicant's "a passivation film formed on the entire surface of the substrate including the source and drain electrodes.").

Thus, claim 5 is rejected.

As to claims 6 and 7, the contact hole of Figure 16 is formed over an edge part of the source electrode and the pixel region adjacent to an edge part of the source electrode.

Figure 16, shows the contact hole traced over part of the source electrode and into the pixel region.

Thus, claim 6 and 7 are rejected.

As to claims 8-12 (claim 8 being amended), the method for fabricating the liquid crystal display device would have been obvious in view of the active matrix liquid crystal display device as taught and disclosed in Ono for a display having a bright image and preferable production yield (Abstract and entire patent).

Thus, claims 8-12 are rejected.

Response to Arguments

Applicant's arguments with respect to said claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Patent Examiner
Art Unit 2871

JDG

ANDREW SCHECHTER
PRIMARY EXAMINER